KOE

JDI Group

Kaohsiung Opto-Electronics Inc.

TENTATIVE

FOR MESSRS :_____ DATE : Mar. 29th 2019

TECHNICAL DATA

TX16D205VM0BAA

Contents

ACCEPTED BY:_____ PROPOSED BY: John Chou

2. RECORD OF REVISION

DATE	SHEET No.	SUMMARY

3. GENERAL DATA

3.1 DISPLAY FEATURES

This module is a 6.3” WHVGA of 8:3 format amorphous silicon TFT. The pixel format is vertical stripe and sub pixels are arranged as R (red), G (green), B (blue) sequentially. This display is RoHS compliant, COG (chip on glass) technology and LED backlight are applied on this display.

Part Name	TX16D205VM0BAA
Module Dimensions	167.0(W) mm x 69.0(H) mm x 12.31 (D) mm (With Screw)
LCD Active Area	150.0(W) mm x 52.5(H) mm
Pixel Pitch	0.0625(W) mm x 3 (R.G.B) (W) X0.1875 (H) mm
Resolution	800 x 3(RGB)(W) x 280(H) dots
Color Pixel Arrangement	R, G, B Vertical stripe
LCD Type	Transmissive Color TFT; Normally Black
Display Type	Active Matrix
Number of Colors	262k Colors
Backlight	Light Emitting Diode (LED)
Weight	110g (typ.)
Interface	C-MOS; 18-bit RGB; 50 pins
Power Supply Voltage	3.3V for LCD; 56mA for Backlight (per serial)
Power Consumption	0.35 W for LCD; 1.512 W for Backlight
Viewing Direction	Super Wide Version

4. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage	V_{DD}	-0.3	4	V	-
Input Voltage of Logic	V_I	-0.3	V_{DD}+0.3	V	Note 1
Operating Temperature	Top	-30	85	°C	Note 2
Storage Temperature	Tst	-40	90	°C	Note 2
Backlight Input Current	I_{LED}	-	150	mA	-

Note 1: The rating is defined for the signal voltages of the interface such as PCLK, DE, Hsync, Vsync , XRES, DISP, SLP, RL, TB and RGB data bus.

Note 2: The maximum rating is defined as above based on the chamber temperature, which might be different from ambient temperature after assembling the panel into the application. Moreover, some temperature-related phenomenon as below needed to be noticed:

- Background color, contrast and response time would be different in temperatures other than 25°C.
- Operating under high temperature will shorten LED lifetime.

5. ELECTRICAL CHARACTERISTICS

5.1 LCD CHARACTERISTICS

$T_a = 25\ ^{\circ}C,\ V_{SS} = 0V$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	-	3.0	3.3	3.6	V	-
Input Voltage of Logic	VI	"H" level	$0.7V_{DD}$	-	V_{DD}	V	Note 1
		"L" level	0	-	$0.3V_{DD}$		
Power Supply Current	I_{DD}	V_{DD}=3.3V	-	-	105	mA	Image: All pixels White Note 2
			-	-	0.5	mA	Sleep mode Note 3
Frame Frequency	f_{Frame}	-	-	60	-	Hz	-
CLK Frequency	f_{CLK}	-	18	20	23	MHz	-

Note 1: Rated values indicate operating range of electrical functions.

Note 2: In-rush current is excluded.

Note 3: At the condition of RGB interface signals, TB and RL are fixed to "H" or "L", backlight is turned off, V_{DD}=3.3Vand Ta=25 degree.

5.2 BACKLIGHT CHARACTERISTICS

$T_a = 25\ ^{\circ}C$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
LED Input Voltage	V_{LED}	I_{LED}=56mA	8.1	-	9.0	V	Note1
LED Forward Current (per serial)	I_{LED}	-	-	56	-	mA	
LED Lifetime	-	I_{LED}=56mA	-	50K	-	hrs	Note2

Note 1: Fig.5.1 shows the LED backlight circuit.

Note 2: The estimated lifetime is specified as the time to reduce 50% brightness by applying 56mA / per serial at 25°C.

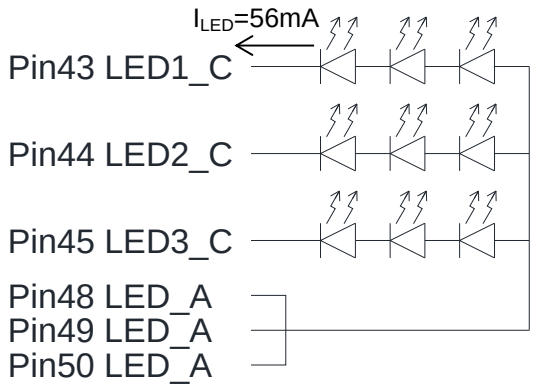


Fig. 5.1

6. OPTICAL CHARACTERISTICS

The optical characteristics are measured based on the conditions as below:

- Supplying the signals and voltages defined in the section of electrical characteristics.
- The backlight unit needs to be turned on for 15 minutes.
- The ambient temperature is 25°C.
- In the dark room around 100~400 lx, the equipment has been set for the measurements as shown in Fig 6.1.

$T_a = 25\ ^{\circ}C,\ f_{Frame} = 60\ \text{Hz},\ V_{DD} = 3.3V$

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Brightness of White		-	$\phi = 0^{\circ}, \theta = 0^{\circ}$, I_{LED}= 56 mA	800	1000	-	cd/m^2	Note 1
Brightness Uniformity		-		70	-	-	%	Note 2
Contrast Ratio		CR		500	1000	-	-	Note 3
Response Time (Rising + Falling)		$T_r + T_f$	$\phi = 0^{\circ}, \theta = 0^{\circ}$	-	40	-	ms	Note 4
NTSC Ratio		-	$\phi = 0^{\circ}, \theta = 0^{\circ}$	-	49	-	%	-
Viewing Angle		θ x	$\phi = 0^{\circ}$, CR ≥ 10	-	85	-	Degree	Note 5
		θ x′	$\phi = 180^{\circ}$, CR ≥ 10	-	85	-		
		θ y	$\phi = 90^{\circ}$, CR ≥ 10	-	85	-		
		θ y′	$\phi = 270^{\circ}$, CR ≥ 10	-	85	-		
Color Chromaticity	Red	X	$\phi = 0^{\circ}, \theta = 0^{\circ}$	0.54	0.59	0.64	-	Note 6
		Y		0.28	0.33	0.38		
	Green	X		0.27	0.32	0.37		
		Y		0.54	0.59	0.64		
	Blue	X		0.10	0.15	0.20		
		Y		0.09	0.14	0.19		
	White	X		0.26	0.31	0.36		
		Y		0.29	0.34	0.39		

Note 1: The brightness is measured from the panel center point, P5 in Fig. 6.2, for the typical value.

Note 2: The brightness uniformity is calculated by the equation as below:

$$\text{Brightness uniformity} = \frac{\text{Min. Brightness}}{\text{Max. Brightness}} \times 100\%$$

, which is based on the brightness values of the 9 points measured by BM-5 or equivalent as shown in Fig. 6.2.

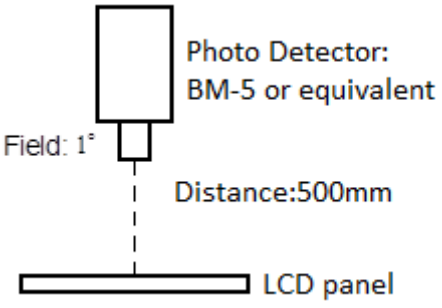


Fig. 6.1

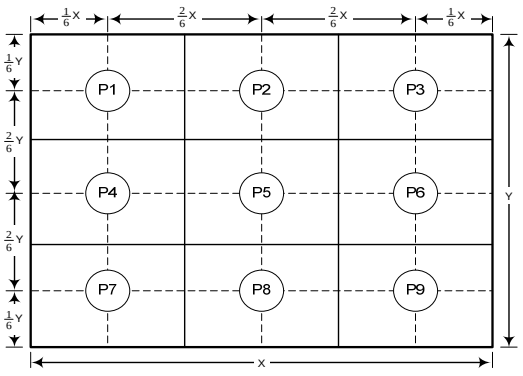


Fig. 6.2

Note 3: The contrast ratio is measured from the center point of the panel, P5, and defined as the following equation:

$$CR = \frac{\text{Brightness of White}}{\text{Brightness of Black}}$$

Note 4: The definition of response time is shown in Fig. 6.3. The rising time is the period from 10% brightness to 90% brightness when the data is from black to white. Oppositely, falling time is the period from 90% brightness rising to 10% brightness.

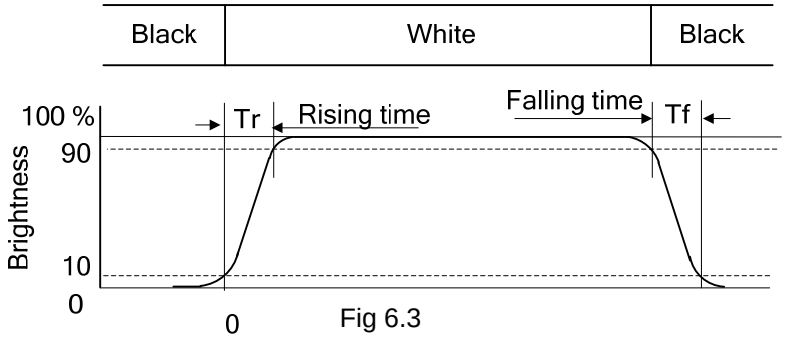


Fig 6.3

Note 5: The definition of viewing angle is shown in Fig. 6.4. Angle ϕ is used to represent viewing directions, for instance, $\phi = 270^\circ$ means 6 o'clock, and $\phi = 0^\circ$ means 3 o'clock. Moreover, angle θ is used to represent viewing angles from axis Z toward plane XY.

The display is super wide viewing angle version, so that the best optical performance can be obtained from every viewing direction.

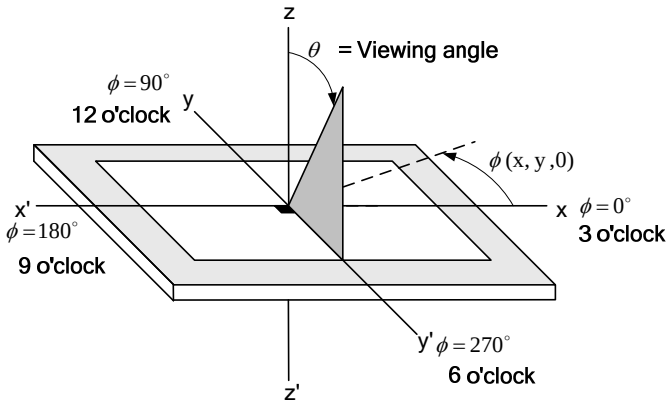
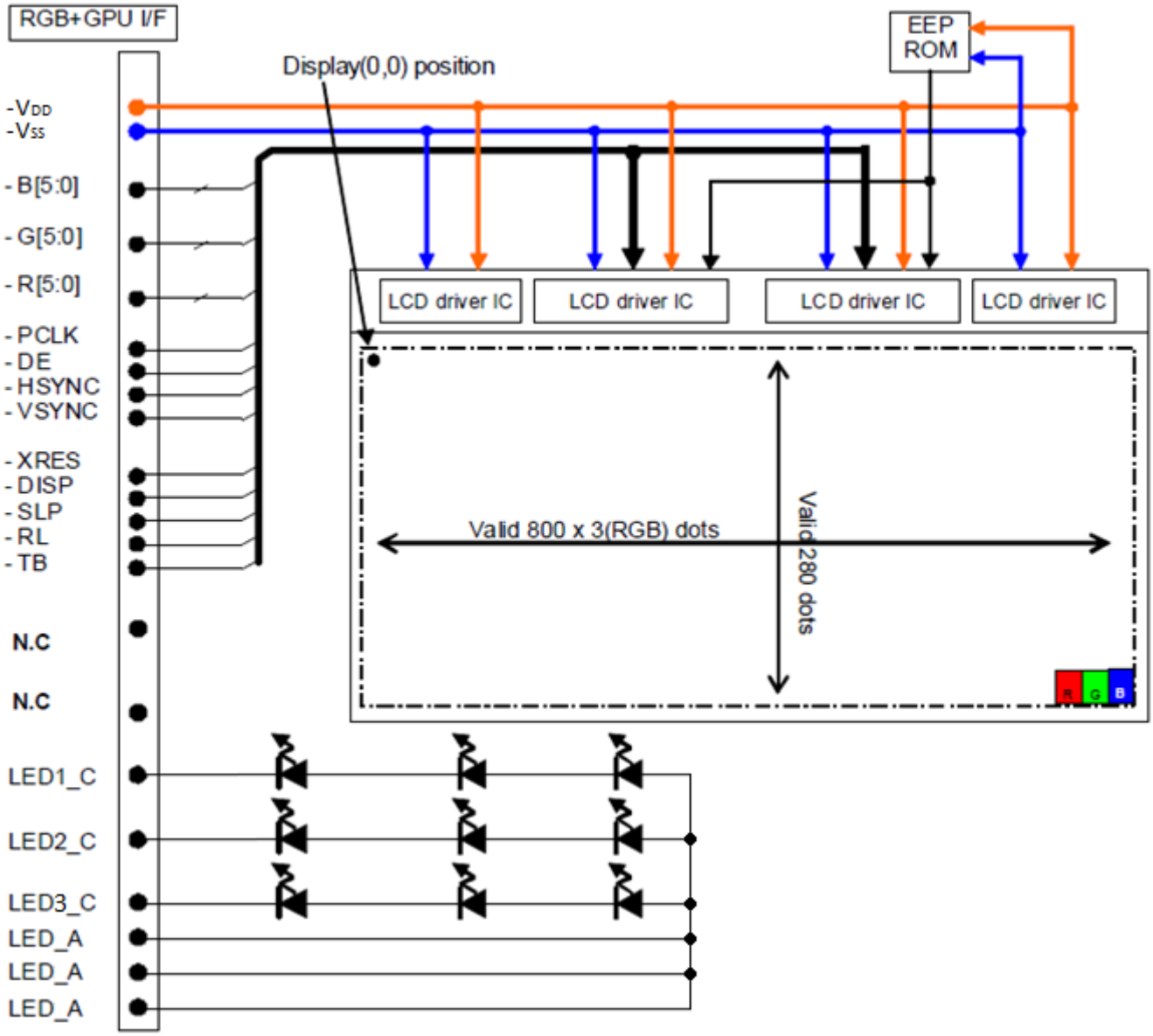


Fig 6.4

Note 6: The color chromaticity is from the center point of panel, P5, as shown in Fig. 6.2.

7. BLOCK DIAGRAM



Note1: Signals are PCLK, DE, Hsync, Vsync, XRES, DISP, SLP, RL, TB and RGB data bus.

8. LCD INTERFACE

8.1 INTERFACE PIN CONNECTIONS

Pin assignment is as below:

Pin No.	Signal	I/O	Function
1	V_{DD}	P	Power Supply
2	V_{DD}	P	Power Supply
3	V_{SS}	P	Ground
4	V_{SS}	P	Ground
5	B5	I	Blue Data (MSB)
6	B4	I	Blue Data
7	B3	I	
8	B2	I	
9	B1	I	
10	B0	I	Blue Data (LSB)
11	V_{SS}	P	Ground
12	G5	I	Green Data (MSB)
13	G4	I	Green Data
14	G3	I	
15	G2	I	
16	G1	I	
17	G0	I	Green Data (LSB)
18	V_{SS}	P	Ground
19	R5	I	Red Data (MSB)
20	R4	I	Red Data
21	R3	I	
22	R2	I	
23	R1	I	
24	R0	I	Red Data (LSB)
25	V_{SS}	P	Ground
26	V_{SS}	P	Ground
27	PCLK	I	Pixel clock signal.
28	V_{SS}	P	Ground
29	V_{SS}	P	Ground
30	DE	I	Data Enable
31	HSYNC	I	Horizontal synchronous signal. This signal is active “L”.
32	VSYNC	I	Vertical synchronous signal. This signal is active “L”.

Pin No.	Signal	I/O	Function
33	V_{SS}	P	Ground
34	XRES	I	Display is initialized when XRES is set to “L”.
35	V_{SS}	P	Ground
36	DISP	I	Display on and off control. “H” Display on. “L” Display off.
37	SLP	I	Booster on and off control. “H” LCD internal power on. “L” LCD internal power off. Please do not change input level for this terminal while operating.
38	RL	I	Horizontal scanning direction selection pin. “H” Left to Right. “L” Right to Left.
39	TB	I	Vertical scanning direction selection pin “H” TOP to Bottom. “L” Bottom to Top.
40	NC	-	No Connection
41	NC	-	No Connection
42	V_{SS}	P	Ground
43	LED1_C	P	LED cathode 1
44	LED2_C	P	LED cathode 2
45	LED3_C	P	LED cathode 3
46	NC	-	No Connection
47	NC	-	No Connection
48	LED_A	P	LED anode
49	LED_A	P	LED anode
50	LED_A	P	LED anode

8.2 TIMING CHART

A. RGB interface timing

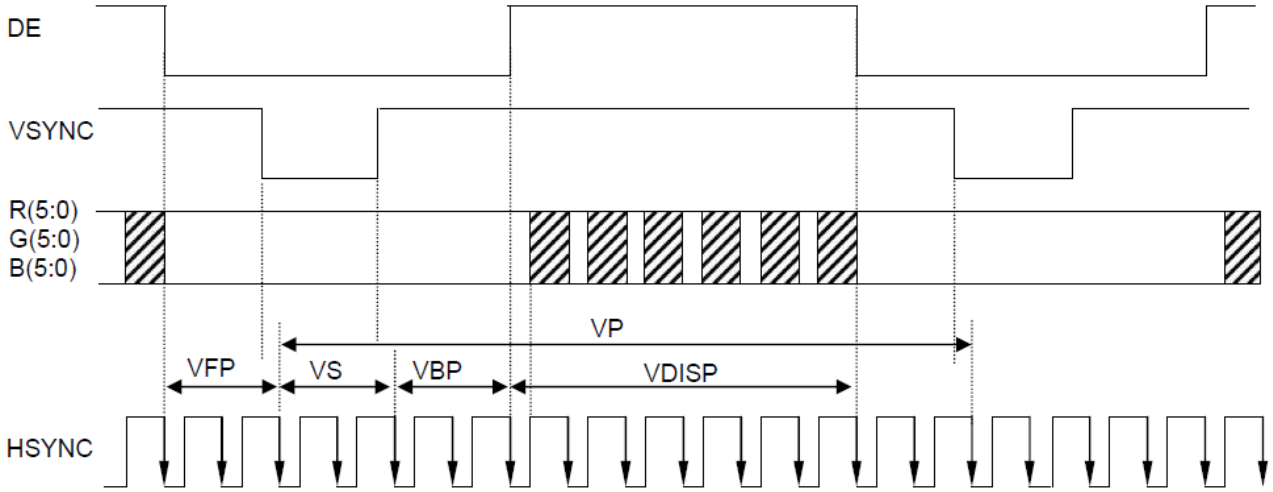


Fig. 8.1 Vertical Timing

Signal	Parameter	MIN	TYP	MAX	Unit	Description
VP	Vertical cycle	315	315	315	Line	*1, *2, *3
VS	Vertical “L” pulse width	12	12	12	Line	
VBP	Vertical back porch	16	16	16	Line	
VFP	Vertical front porch	7	7	7	Line	
VDISP	Vertical active area	280	280	280	Line	
VRR	Frame rate		60		Hz	*4

*1 The rise and fall times of all input signals (tr, tf) are equal or less than 8ns.
*2 For timing of input signals, they are set using 30 % and 70 % of V_{DD} as the base reference.
*3 Number of line is counted an inputted HSYNC falling edge after VSYNC signal is changed.
*4 LCD frame rate should be adjusted 60Hz by porch clock numbers. See 4.2.1 (2).
*5 There is no tolerance for VP,VS,VBP,VFP,VDISP. Please use fixed value.

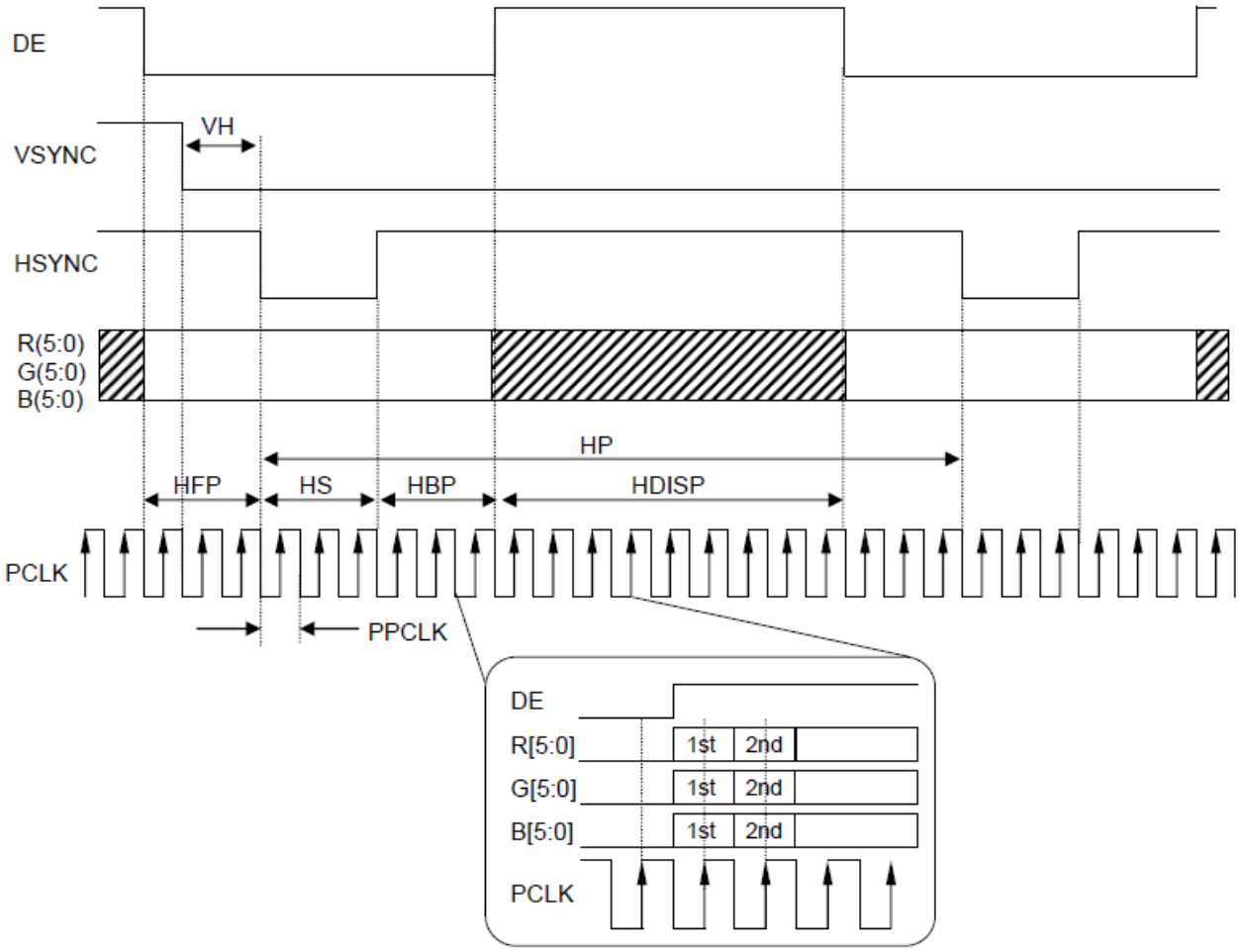


Fig. 8.2 Horizontal Timing

Signal	Parameter	MIN	TYP	MAX	Unit	Description
VH	Phase difference of VSYNC-HSYNC	0	-	898	PCLK	*3
HP	Horizontal cycle	960	1056	1224	PCLK	*1, *2
HS	Horizontal “L” pulse width	80	128	128	PCLK	
HBP	Horizontal back porch	56	88	256	PCLK	
HFP	Horizontal front porch	24	40	40	PCLK	
HDISP	Horizontal active area	800	800	800	PCLK	
f_{PCLK}	Pixel clock frequency	18	20	23	MHz	
PPCLK		43.47	50	55	ns	

*1 The rise and fall times of all input signals (tr, tf) are equal or less than 8ns.
*2 For timing of input signals, they are set using 30 % and 70 % of V_{DD} as the base reference.
*3 VH Max value is HP(Horizontal cycle)-62.

B. CLOCK AND DATA INPUT TIMING

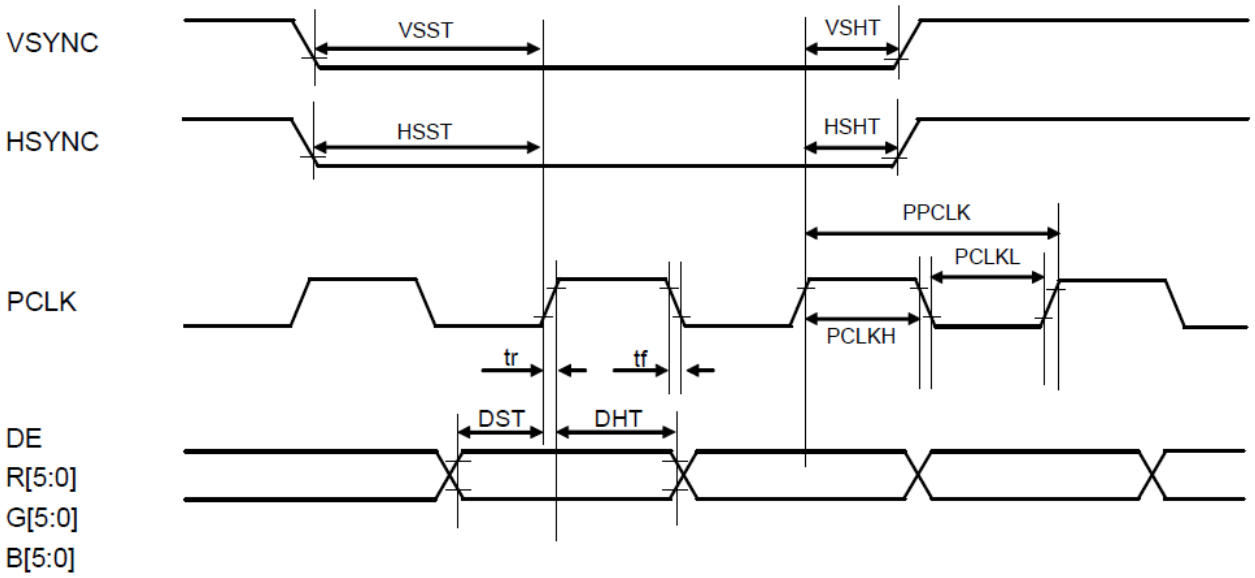


Fig. 8.3 Setup & Hold Time of Data, DE signal, Hsync and Vsync signal.

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
VSYNC	VSST	VSYNC set up time	10	-	-	ns	
	VSHT	VSYNC hold time	10	-	-	ns	
HSYNC	HSST	HSYNC set up time	10	-	-	ns	
	HSHT	HSYNC hold time	10	-	-	ns	
PCLK	PPCLK	Pixel clock period	43.47	-	-	ns	
	PCLKL	Pixel clock low time	14	-	-	ns	*1, *2
	PCLKH	Pixel clock high time	14	-	-	ns	
DE R[5:0] G[5:0] B[5:0]	DST	Data setup time	10	-	-	ns	
	DHT	Data hold time	10	-	-	ns	

*1 The rise and fall times of all input signals (tr, tf) are equal or less than 8ns.
*2 For timing of all input signals, they are set using 30 % and 70 % of V_{DD} as the base reference.

C. RESET TIMING

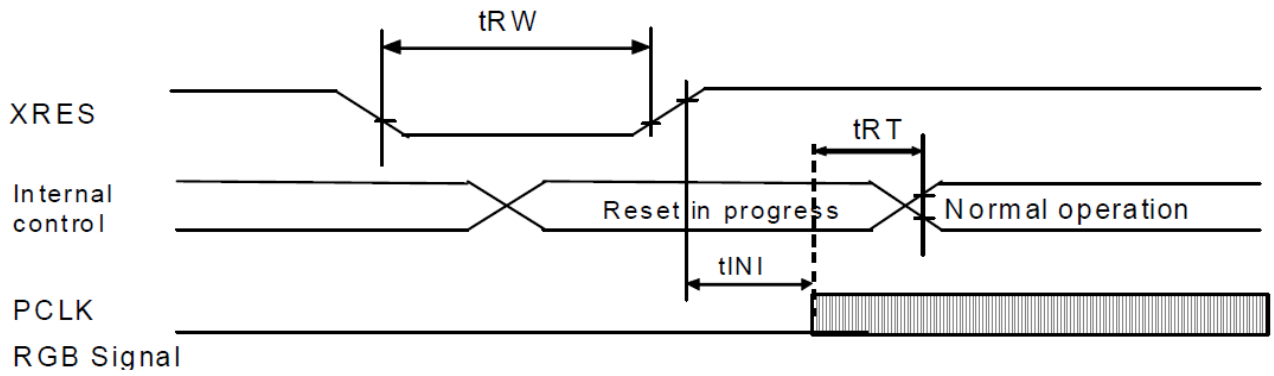


Fig. 8.4 Reset timing

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
XRES	tRW	reset pulse width	20	-	us	*1
	tINI	initial start	1	-	ms	*2, *3
	tRT	Clear reset	-	10	ms	*1, *2

*1 The rise and fall times of the input signal (tr, tf) are equal or less than 15ns.
For all timings are set using 30 % and 70 % of V_{DD}-V_{SS} as the base reference.
*2 It must be avoid to transfer the GPU IF terminals for this period.
*3 It is necessary to avoid input PCLK and RGB signals at this period.

8.3 RECOMMENDED SEQUENCE

Power ON

(1) Start to supply system power (V_{DD}).
(2) Make a device reset after starting to supply the system power.
(XRES must be kept "L" for more than 20us to less than 200ms.)
(3) Wait more than 1ms to less than 10ms after releasing the system reset.
(4) Input logic signals (PCLK, HSYNC, VSYNC, DE and RGB data).
(5) Wait more than 10ms after input logic signals.
(6) Transfer “L” to “H” of SLP signal. (Internal power is started.)
(7) TB and RL signals are fixed in the direction of display, if necessary.
(8) Backlight turns on.

Power OFF

(9) Backlight turns off.
(10) Transfer “H” to “L” of SLP signal. (Internal power and display is stopped.)
(11) Wait more than 50 ms, then transfer “H” to “L” of DISP signal.
(12) Wait more than 250 ms, then XRES signal turns “L” state.
(13) Stop to supply system power（V_{DD}）.

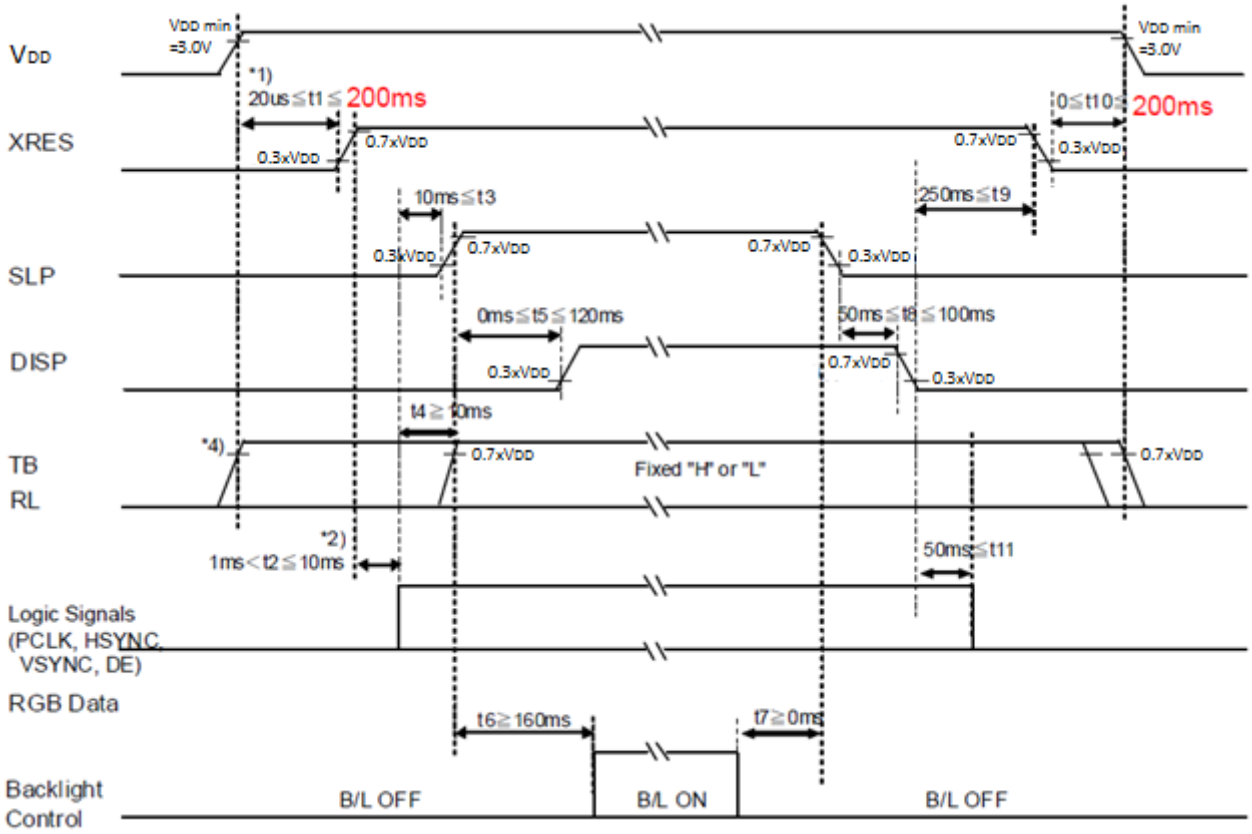


Fig. 8.5 Recommended sequence

Notes)

* 1 XRES must be maintained to “LOW” more than 20us after turning on the system power (V_{DD}).
* 2 Logic signals should be start more than 1 ms after XRES signal is released.
* 3 The rising speed of V_{DD} should be less than 2V/100us.
* 4 TB and RL signals allow fix the V_{DD} or V_{SS}.

8.4 INTERVAL POWER ON AND OFF

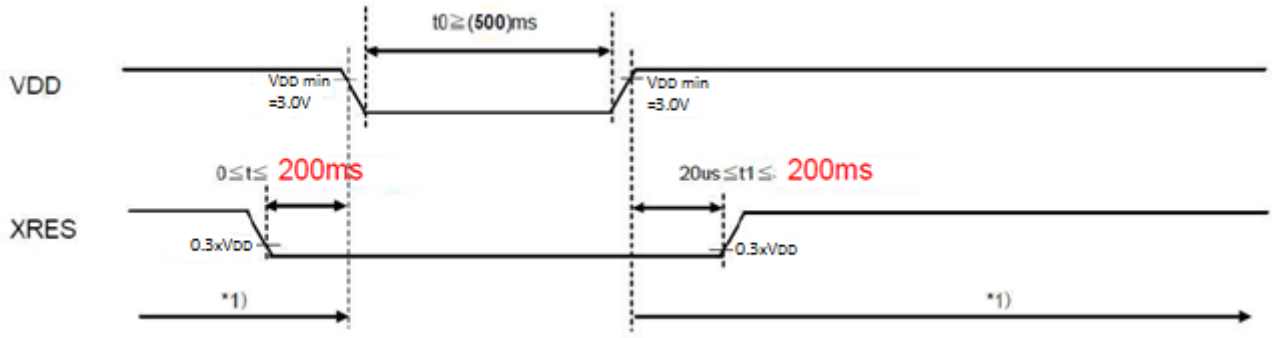


Fig. 8.6 Interval Power on/off Timing

Notes)

* 1 Please refer to 8.3 RECOMMENDED SEQUENCE when system power(V_{DD}) is stopped and when after system power(V_{DD}) is running.

8.5 TRANSITION OF POWER MODE

This module has three power modes as following.

a) SLEEP MODE : Internal power OFF, LCD driving is OFF in this mode.

b) DISPLAY ON MODE : Internal power ON, LCD driving is ON in this mode.

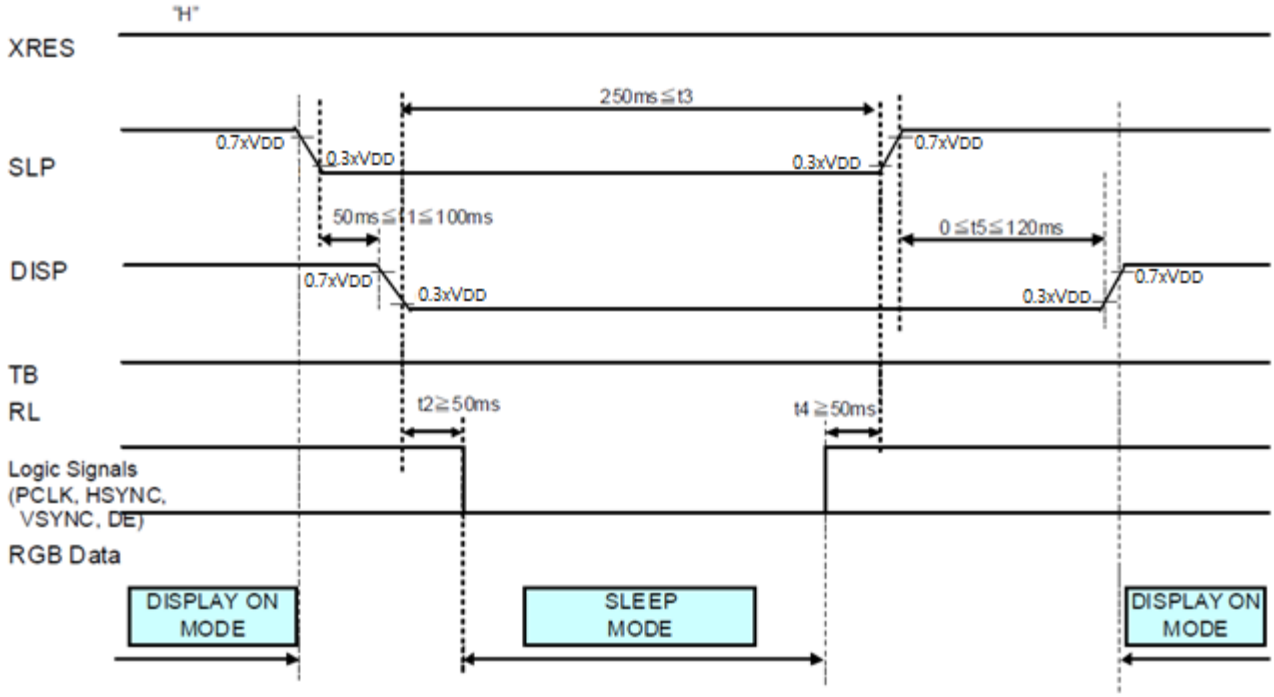


Fig. 8.7 Power Transition Timing

8.6 GPU INTERFACE

Display control is possible by using the following 4 terminals: DISP, SLP, TB and RL.

Terminal	Description
DISP	Display on and off control. H : display on. L : display off.
SLP	Booster on and off control. H : LCD internal power on. L : LCD internal power off.
TB	Vertical scanning direction selection pin. H : Top to bottom L : Bottom to top
RL	Horizontal scanning direction selection pin. H : Left to right L : Right to left.

See 8.3 RECOMMENDED SEQUENCE to design a sequence and intervals.

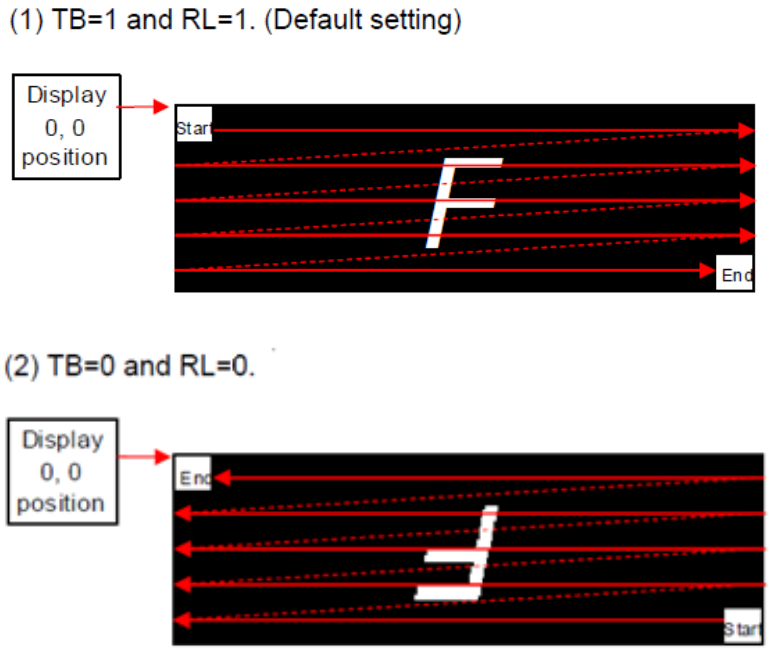


Fig. 8.8 Scanning direction selection

8.7 DATA INPUT for DISPLAY COLOR

	COLOR & Gray Scale	Data Signal																	
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red (62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
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	Green (61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green (62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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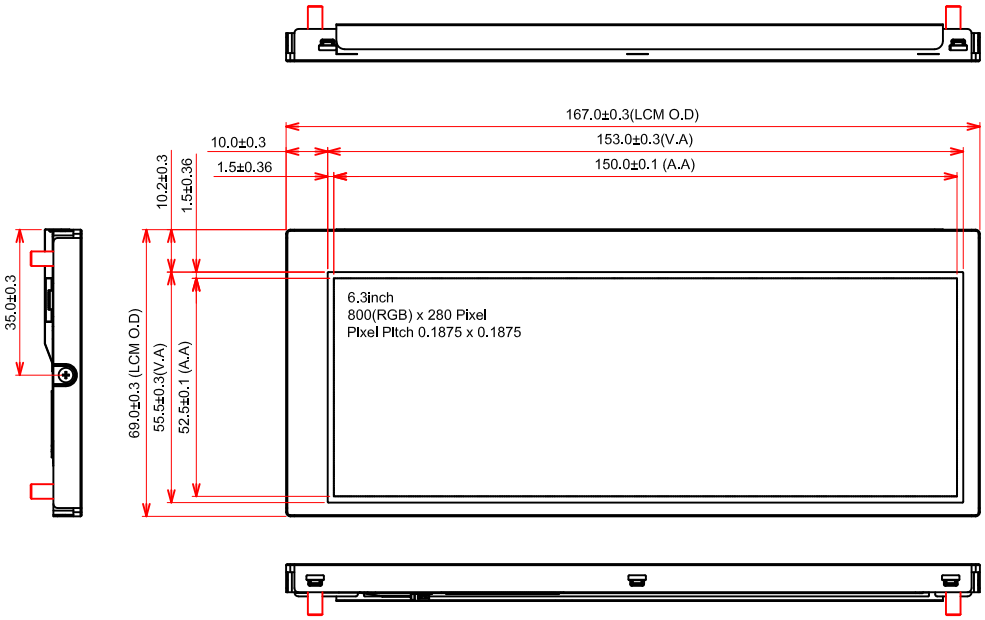
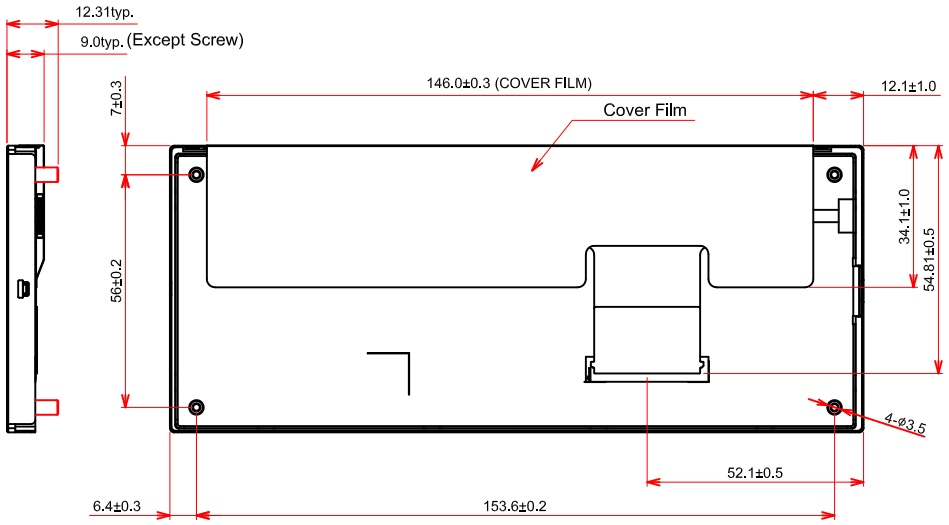
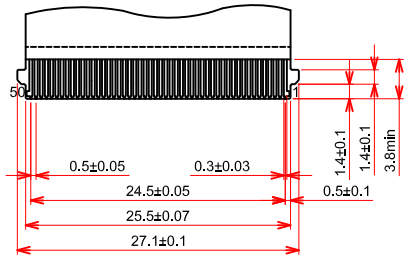
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue (62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

9. OUTLINE DIMENSIONS







Detail I/F

General
Tolerance:±0.5mm
Scale : NTS
Unit : mm

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10. DESIGNATION of LOT MARK

1) The lot mark is showing in Fig.10.1. First 4 digits are used to represent production lot, T represented made in Taiwan, and the last 6 digits are the serial number.

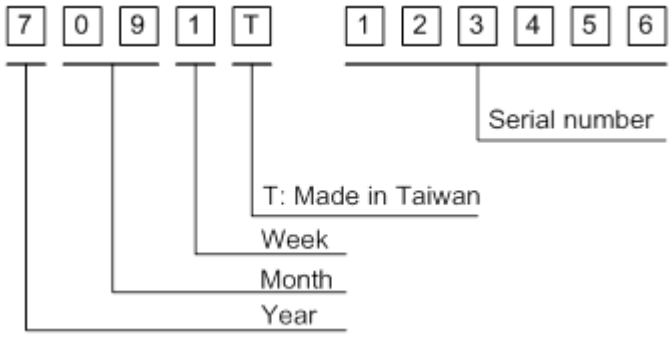

Fig. 10.1

2) The tables as below are showing what the first 4 digits of lot mark are shorted for.

Year	Lot Mark
2019	9
2020	0
2021	1
2022	2
2023	3

Month	Lot Mark	Month	Lot Mark
Jan.	01	Jul.	07
Feb.	02	Aug.	08
Mar.	03	Sep.	09
Apr.	04	Oct.	10
May	05	Nov.	11
Jun.	06	Dec.	12

Week	Lot Mark
1~7 days	1
8~14 days	2
15~21 days	3
22~28 days	4
29~31 days	5

3) The location of the lot mark is on the back of the display shown in Fig. 10.2

Label example :

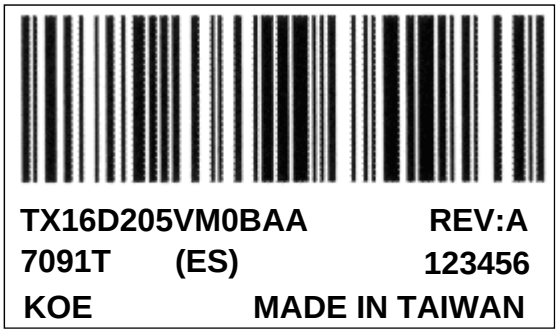

Fig. 10.2