TENTATIVE

KOE

JDI Group

Kaohsiung Opto-Electronics Inc.

FOR MESSRS : _____ DATE : Oct. 26th ,2017

TECHNICAL DATA

TX16D201VM0BAB

Contents

ACCEPTED BY: _____ PROPOSED BY: Jolin Chou

2. RECORD OF REVISION

DATE	SHEET No.	SUMMARY

3. GENERAL DATA

3.1 DISPLAY FEATURES

This module is a 6.4” XGA of 4:3 format LTPS TFT. The pixel format is vertical stripe and sub pixels are arranged as R (red), G (green), B (blue) sequentially. This display is RoHS compliant, COG (chip on glass) technology and LED backlight are applied on this display that made in Taiwan.

Part Name	TX16D201VM0BAB
Module Dimensions	153.0(W) mm x 118.0(H) mm x 8.7 (D) mm typ.
LCD Active Area	129.792(W) mm x 97.344(H) mm
Pixel Pitch	0.126(W) mm x 0.126 (H) mm
Resolution	1024 x 3(RGB)(W) x 768(H) dots
Color Pixel Arrangement	R, G, B Vertical stripe
LCD Type	LTPS TFT; Transmissive Normally Black
Top Polarizer Type	Anti-glare Polarizer Film
Display Type	Active Matrix
Number of Colors	16.7M Colors (8-bit RGB)
Backlight	Light Emitting Diode(LED)
Weight	190g typ.
Interface	LVDS; 20 pins
Power Supply Voltage	3.3V for LCD; 12V for Backlight
Power Consumption	0.231 W for LCD; 4.56 W for Backlight
Viewing Direction	Super Wide Version (In-Plane Switching)

4. ABSOLUTE MAXIMUM RATINGS

4.1 ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage	V_{DD}	-0.3	4.5	V	-
Input Voltage of Logic	V_I	-0.3	V_{DD}	V	Note 1
Operating Temperature	Top	-30	80	°C	Note 2
Storage Temperature	Tst	-30	80	°C	Note 2
Backlight Input Voltage	V_L	0	15	V	-

Note 1: The rating is defined for the signal voltages of the interface such as CLK and pixel data pairs.

Note 2: The maximum rating is defined as above based on the chamber temperature, which might be different from ambient temperature after assembling the panel into the application. Moreover, some temperature-related phenomenon as below needed to be noticed:

- Background color, contrast and response time would be different in temperatures other than 25°C.
- Operating under high temperature will shorten LED lifetime.

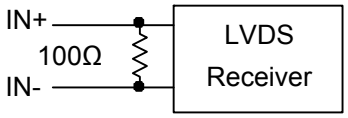
5. ELECTRICAL CHARACTERISTICS

5.1 LCD CHARACTERISTICS

$T_a = 25\ ^\circ C,\ V_{SS} = 0V$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	-	3.0	3.3	3.6	V	-
Differential Input Voltage for LVDS Receiver Threshold	V_I	"H" level	$0.7V_{DD}$	-	V_{DD}	mV	Note 1
		"L" level	V_{SS}	-	$0.3V_{DD}$		
Power Supply Current	I_{DD}	V_{DD}=3.3V	-	70	-	mA	Note 2
Frame Frequency	f_{Frame}	-	55	60	65	Hz	-
CLK Frequency	f_{CLK}	-	-	56.3	-	MHz	-
Input Voltage of Logic	V_I	"H" level	2.1	-	3.6	V	-
		"L" level	0	-	0.5		

Note 1: VCM 1.2V is common mode voltage of LVDS transmitter and receiver. The input terminal of LVDS transmitter is terminated with 100Ω.



Note 2: An all white check pattern is used when measuring I_{DD}. f_{Frame} is set to 60 Hz. Moreover, 0.5A fuse is applied in the module for I_{DD}. For display activation and protection purpose, power supply is recommended larger than 1.25A to start the display and break fuse once any short circuit occurred.

5.2 BACKLIGHT CHARACTERISTICS

$T_a = 25\ ^\circ C$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
LED Input Voltage	V_L	-	10.8	12.0	13.2	V	Note1
LED Forward Current (Dim Control)	I_L	0% duty	350	380	420	mA	Note 2
		100% duty	-	10	-		
LED lifetime	-	I_{LED}= 380 mA	-	70K	-	hrs	Note 3

Note 1: As Fig. 5.1 shown, LED current is constant, 380 mA, controlled by the LED driver when applying 12V.

Note 2: Dimming function can be obtained by applying PWM signal from the display interface DIM (No.6pin) of CN2. The recommended PWM signal is 200Hz ~ 1K Hz with 3.3V amplitude.

Note 3: The estimated lifetime is specified as the time to reduce 50% brightness by applying 380 mA at 25°C.

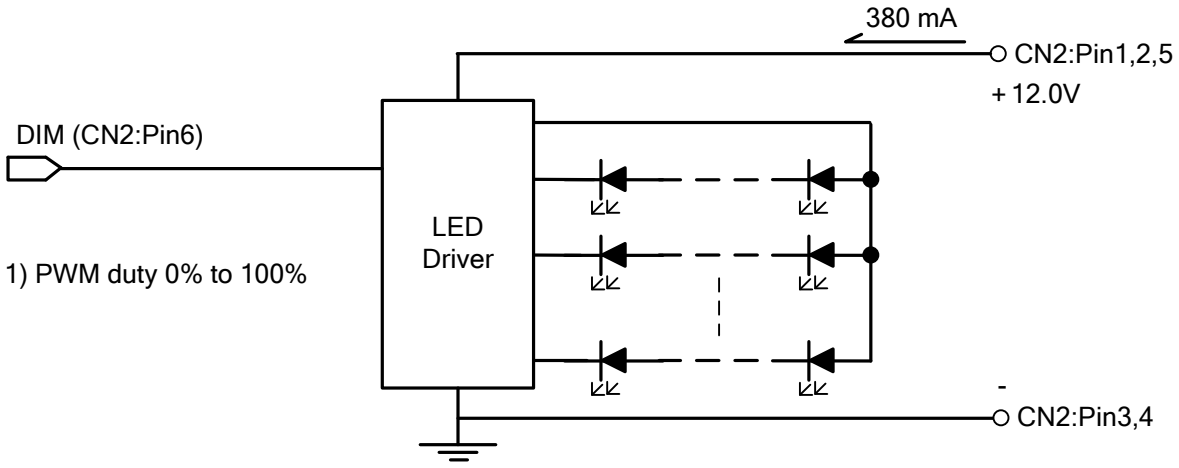


Fig. 5.1

6. OPTICAL CHARACTERISTICS

The optical characteristics are measured based on the conditions as below:

- Supplying the signals and voltages defined in the section of electrical characteristics.
- The backlight unit needs to be turned on for 30 minutes.
- The ambient temperature is 25°C.
- In the dark room less than 100lx, the equipment has been set for the measurements as shown in Fig 6.1.

$T_a = 25\,^{\circ}C,\ f_{Frame} = 60\,\text{Hz}, V_{DD} = 3.3\text{V}$

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Brightness of White		-	$\phi = 0^{\circ}, \theta = 0^{\circ}$, I_{LED}= 380 mA	-	1400	-	cd/m^2	Note 1
Brightness Uniformity		-		75	-	-	%	Note 2
Contrast Ratio		CR		-	800	-	-	Note 3
Response Time		$T_r + T_f$	$\phi = 0^{\circ}, \theta = 0^{\circ}$	-	30	-	ms	Note 4
NTSC Ratio		-	$\phi = 0^{\circ}, \theta = 0^{\circ}$	-	60	-	%	-
Viewing Angle		θx	$\phi = 0^{\circ}$, CR ≥ 10	-	85	-	Degree	Note 5
		$\theta x'$	$\phi = 180^{\circ}$, CR ≥ 10	-	85	-		
		θy	$\phi = 90^{\circ}$, CR ≥ 10	-	85	-		
		$\theta y'$	$\phi = 270^{\circ}$, CR ≥ 10	-	85	-		
Color Chromaticity	Red	X	$\phi = 0^{\circ}, \theta = 0^{\circ}$	-	0.62	-	-	Note 6
		Y		-	0.33	-		
	Green	X		-	0.32	-		
		Y		-	0.58	-		
	Blue	X		-	0.16	-		
		Y		-	0.08	-		
	White	X		-	0.31	-		
		Y		-	0.33	-		

Note 1: The brightness is measured from the panel center point, P5 in Fig. 6.2, for the typical value.

Note 2: The brightness uniformity is calculated by the equation as below:

$$\text{Brightness uniformity} = \frac{\text{Min. Brightness}}{\text{Max. Brightness}} \times 100\%$$

, which is based on the brightness values of the 9 points measured by BM-5 as shown in Fig. 6.2.

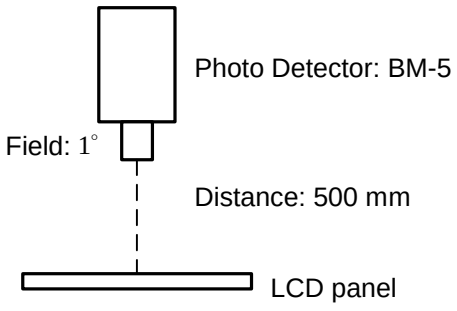


Fig. 6.1

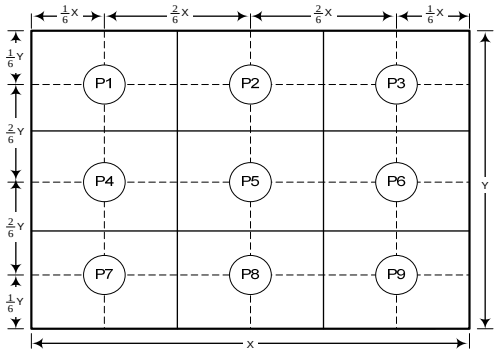


Fig. 6.2

Note 3: Continuously operating the test pattern (see below chess pattern Fig.6.3) on display for 2 hours at 25℃ then switch to completely white pattern, the previous test pattern shall disappear within 2 seconds.

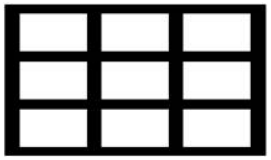


Fig.6.3

Note 4: The Contrast Ratio is measured from the center point of the panel, P5, and defined as the following equation:

$$CR = \frac{\text{Brightness of White}}{\text{Brightness of Black}}$$

Note 5: The definition of response time is shown in Fig. 6.4. The rising time is the period from 10% brightness to 90% brightness when the data is from black to white. Oppositely, Falling time is the period from 90% brightness falling to 10% brightness.

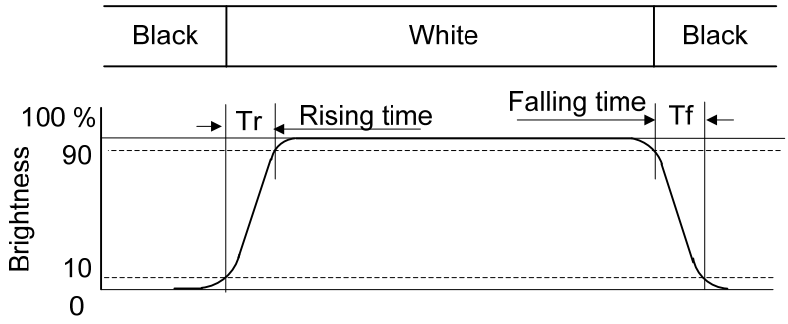


Fig.6.4

Note 6: The definition of viewing angle is shown in Fig. 6.5. Angle ϕ is used to represent viewing directions, for instance, $\phi = 270^\circ$ means 6 o'clock, and $\phi = 0^\circ$ means 3 o'clock. Moreover, angle θ is used to represent viewing angles from axis Z toward plane XY.

The display is super wide viewing angle version, so that the best optical performance can be obtained from every viewing direction.

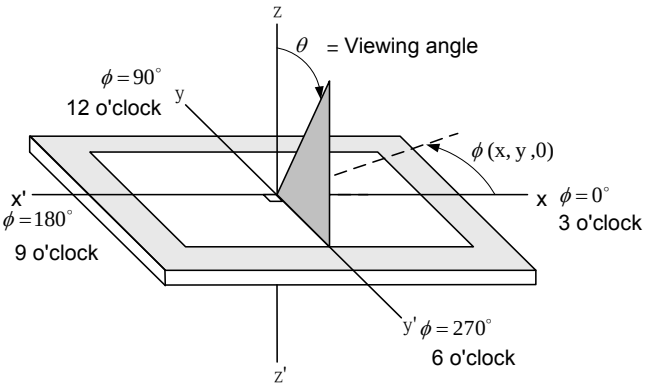
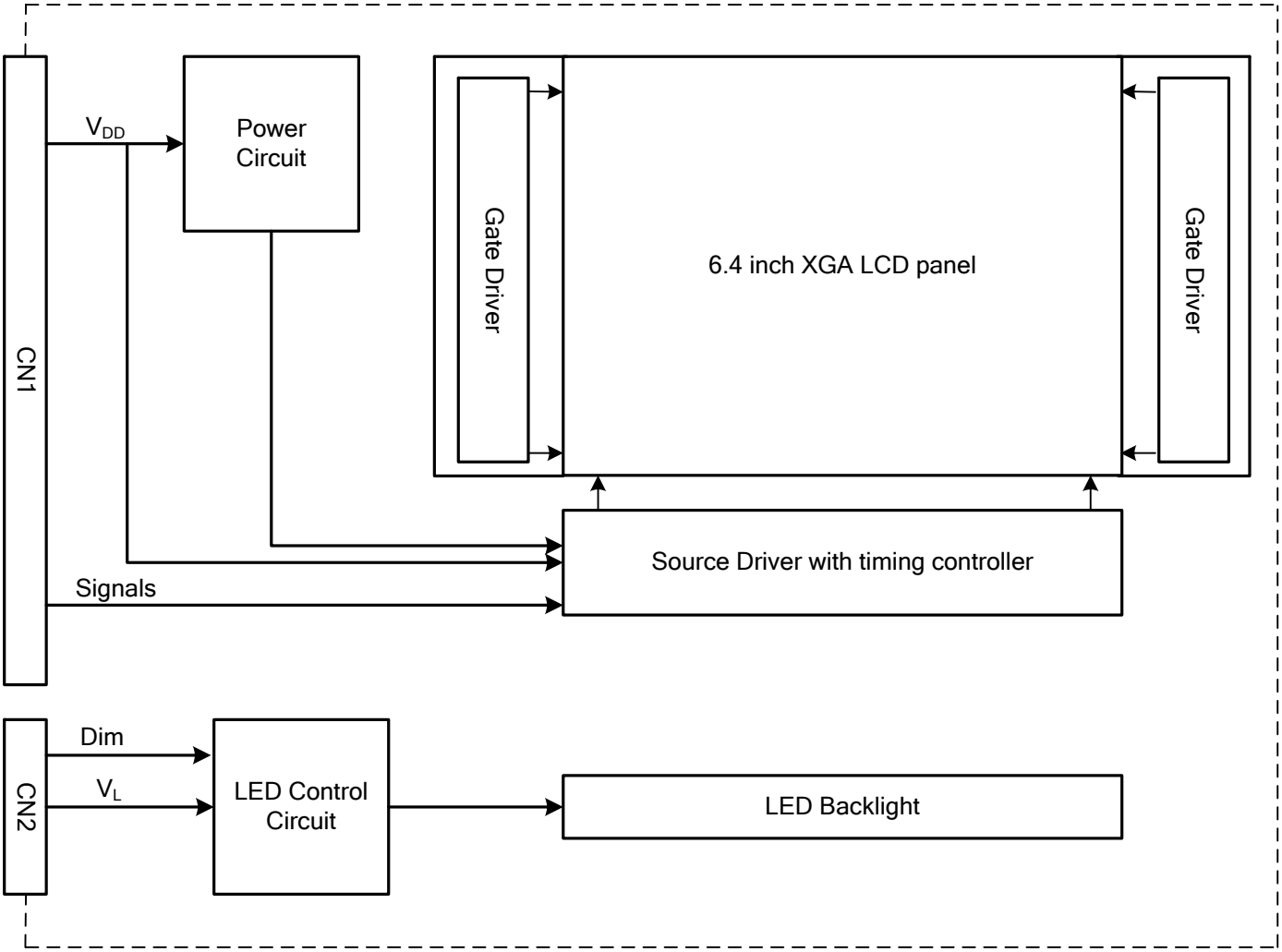


Fig 6.5

Note 7: The color chromaticity is measured from the center point of the panel, P5, as shown in Fig. 6.2.

7. BLOCK DIAGRAM



Note 1: Signals are SD, AMODE, CLK and pixel data pairs.

8. LCD INTERFACE

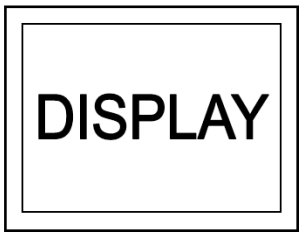
8.1 INTERFACE PIN CONNECTIONS

The display interface connector (CN1) is DF14H-20P-1.25H made by HIROSE and pin assignment is as below:

Pin No.	Symbol	Signal	Pin No.	Symbol	Signal
1	V_{DD}	Power Supply for Logic	11	IN2-	Pixel Data
2	V_{DD}		12	IN2+	
3	V_{SS}	GND	13	V_{SS}	GND
4	V_{SS}		14	CLK IN-	Pixel Clock
5	IN0-	Pixel Data	15	CLK IN+	
6	IN0+		16	V_{SS}	GND
7	V_{SS}	GND	17	IN3-	Pixel Data
8	IN1-	Pixel Data	18	IN3+	
9	IN1+		19	SD	Scan Direction Control (Note 2)
10	V_{SS}	GND	20	AMODE	Open / L:JEIDA, H:VESA

Note 1: IN n- and IN n+ (n=0, 1, 2, 3), CLK IN- and CLK IN+ should be wired by twist-pairs or side-by-side FPC patterns, respectively.

Note 2: Scan direction is available to be switched as below.



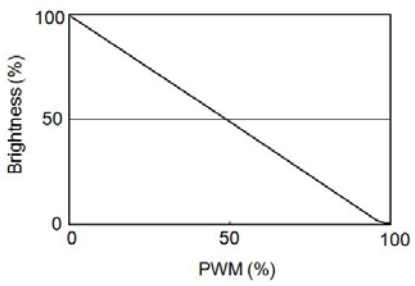
SD：H

SD：L or open

The backlight connector (CN2) is SM06B-SHLS-TF, and pin assignment is as below:

Pin No.	Signal	Signal
1	V_{LED}	12VDC
2	V_{LED}	12VDC
3	GND	Ground
4	GND	Ground
5	V_{LED}	12VDC
6	DIM	3.3V @200Hz~1000Hz

Note 3: The relationship of brightness and Dim control are shown as below.



8.2 TIMING CHART

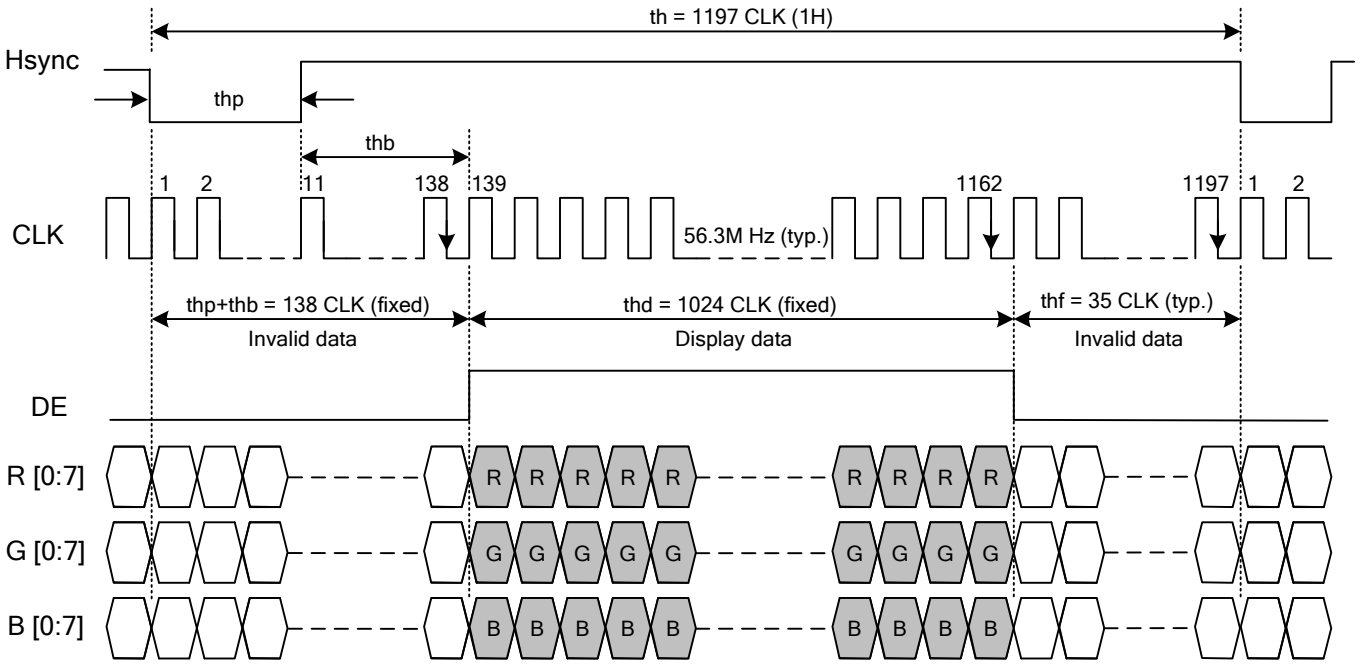


Fig. 8.1 Horizontal Timing of VS-HS-DE Mode

Note 1: CLK's falling edge is the time to latch data and count (thp + thb), therefore, data sending and Hsync's falling edge should start when CLK's rise edge.

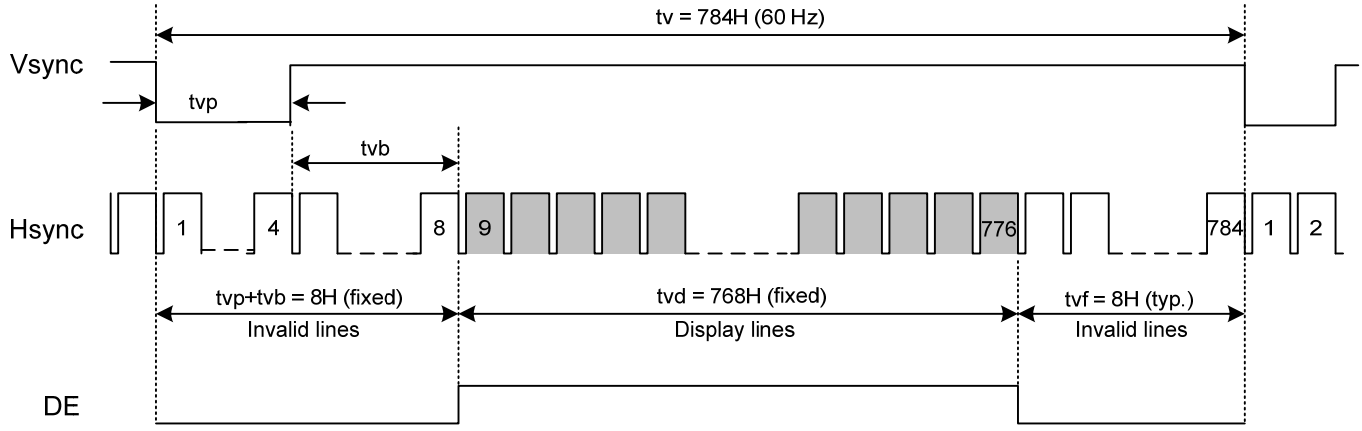
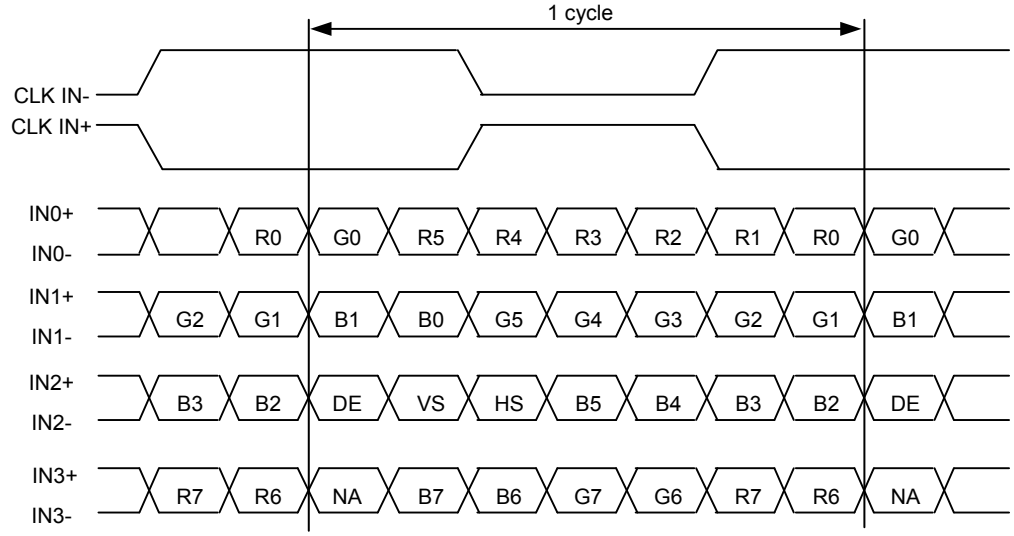


Fig. 8.2 Vertical Timing of VS-HS-DE Mode

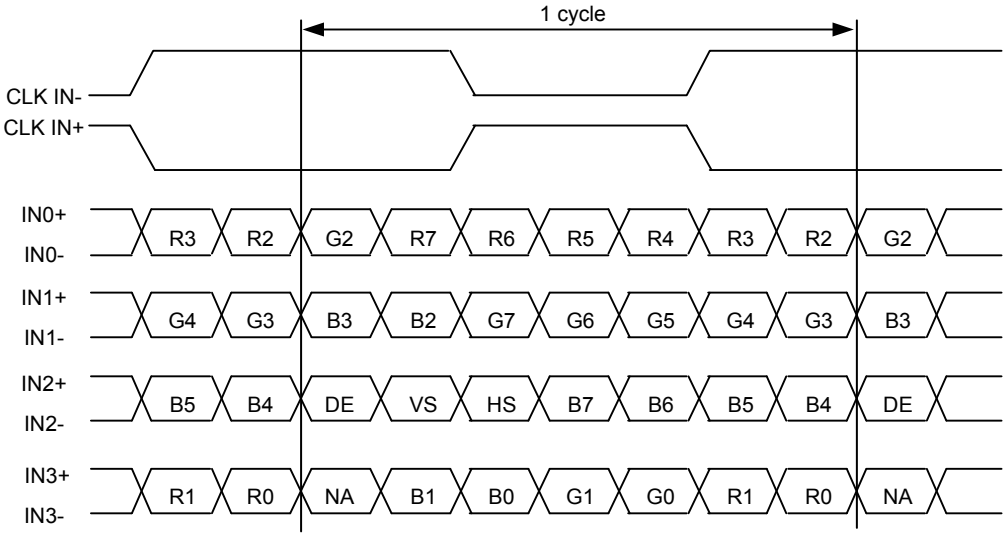
Note 2: Vsync's falling edge needs to start with Hsync's falling edge simultaneously to count (tvp + tvb).

LVDS DATA FORMAT

(1) 8Bit Mode (Amode=H)



(2) 8Bit Mode (Amode=L/Open)



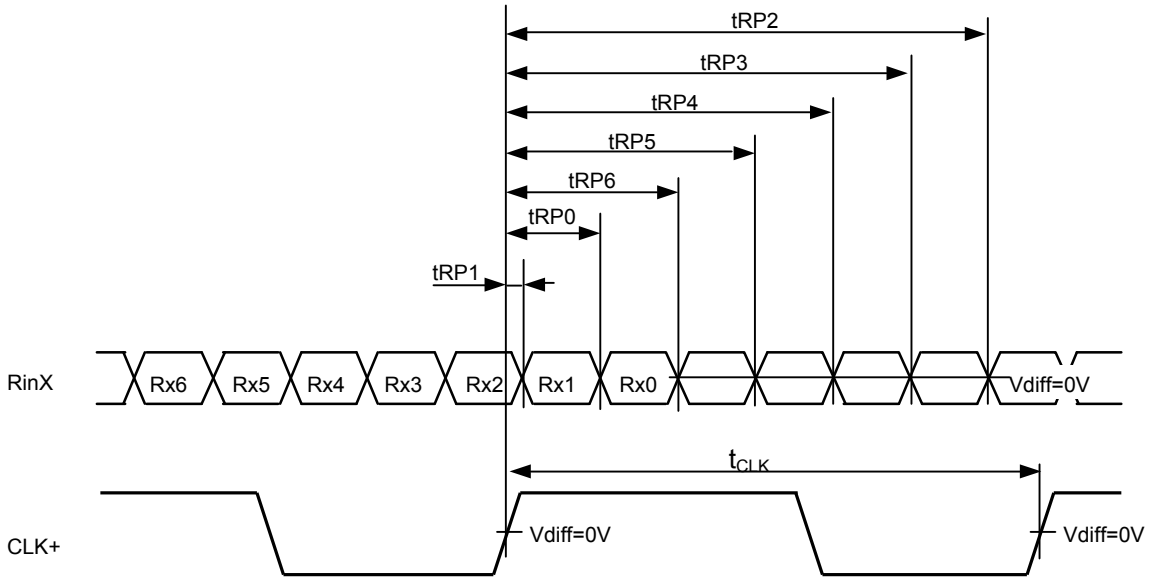
8.3 TIME TABLE

The column of timing sets including minimum, typical, and maximum as below are based on the best optical performance, frame frequency (f_{Frame}) = 60 Hz to define. If 60 Hz is not the aim to set, 55~65 Hz for f_{Frame} is recommended to apply for better performance by other parameter combination as the definitions in section 5.1.

A. HS-VS-DE MODE

Item		Symbol	Min.	Typ.	Max.	Unit
Horizontal	CLK Frequency	fclk	51	56.3	66	M Hz
	Display Data	thd	1024	1024	1024	CLK
	Cycle Time	th	1096	1197	1295	
	Pulse Width	thp	2	10	20	
	Pulse Width and Back Porch	thp + thb	42	138	206	
	Front Porch	thf	30	35	65	
Vertical	Display Line	tvd	768	768	768	H
	Cycle Time	tv	776	784	849	
	Pulse Width	tvp	2	4	10	
	Pulse Width and Back Porch	tvp + tvb	6	8	35	
	Front Porch	tvf	2	8	20	

8.4 LVDS RECEIVER TIMING



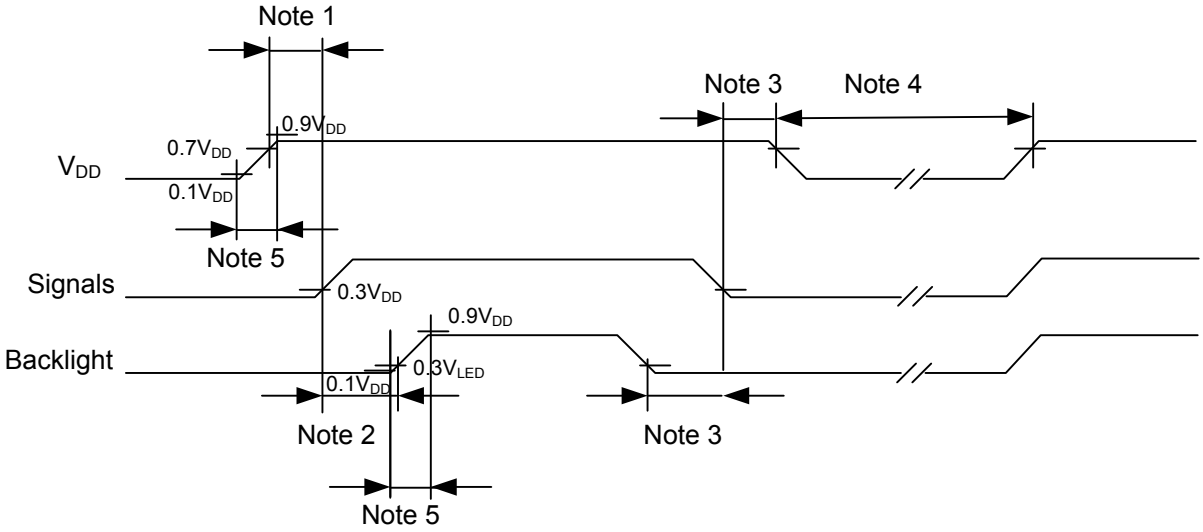
RinX= (RinX+)-(RinX-) (X=0, 1, 2, 3)

Item		Symbol	Min.	Typ.	Max.	Unit
CLK	Cycle frequency	1/tCLK	51	56.3	66	MHz
RinX (X=0,1,2,3)	0 data position	tRP0	1/7* t_{CLK} -0.55	1/7* t_{CLK}	1/7* t_{CLK} +0.55	ns
	1st data position	tRP1	-0.55	0	+0.55	
	2nd data position	tRP2	6/7* t_{CLK} -0.55	6/7* t_{CLK}	6/7* t_{CLK} +0.55	
	3rd data position	tRP3	5/7* t_{CLK} -0.55	5/7* t_{CLK}	5/7* t_{CLK} +0.55	
	4th data position	tRP4	4/7* t_{CLK} -0.55	4/7* t_{CLK}	4/7* t_{CLK} +0.55	
	5th data position	tRP5	3/7* t_{CLK} -0.55	3/7* t_{CLK}	3/7* t_{CLK} +0.55	
	6th data position	tRP6	2/7* t_{CLK} -0.55	2/7* t_{CLK}	2/7* t_{CLK} +0.55	

8.5 DATA INPUT for DISPLAY COLOR

Input color		Red Data								Green Data								Blue Data							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
		MSB							LSB	MSB							LSB	MSB							LSB
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

8.6 POWER SEQUENCE



Note 1: In order to avoid any damages, V_{DD} has to be applied before all other signals. The recommended time period is 1 second (0.2 second is minimum). Hot plugging might cause display damage due to incorrect power sequence, please pay attention on interface connecting before power on.

Note 2: In order to avoid uncompleted patterns in transient state, It is recommended that switching the backlight on is delayed for 1 second after the signals have been applied (0.1 second is minimum).

Note 3: Off sequence is same. The time period from backlight off to signal off and signal off to power off are recommended 1 second. No damage is left if they are turned off simultaneously, but display irregular might be observed.

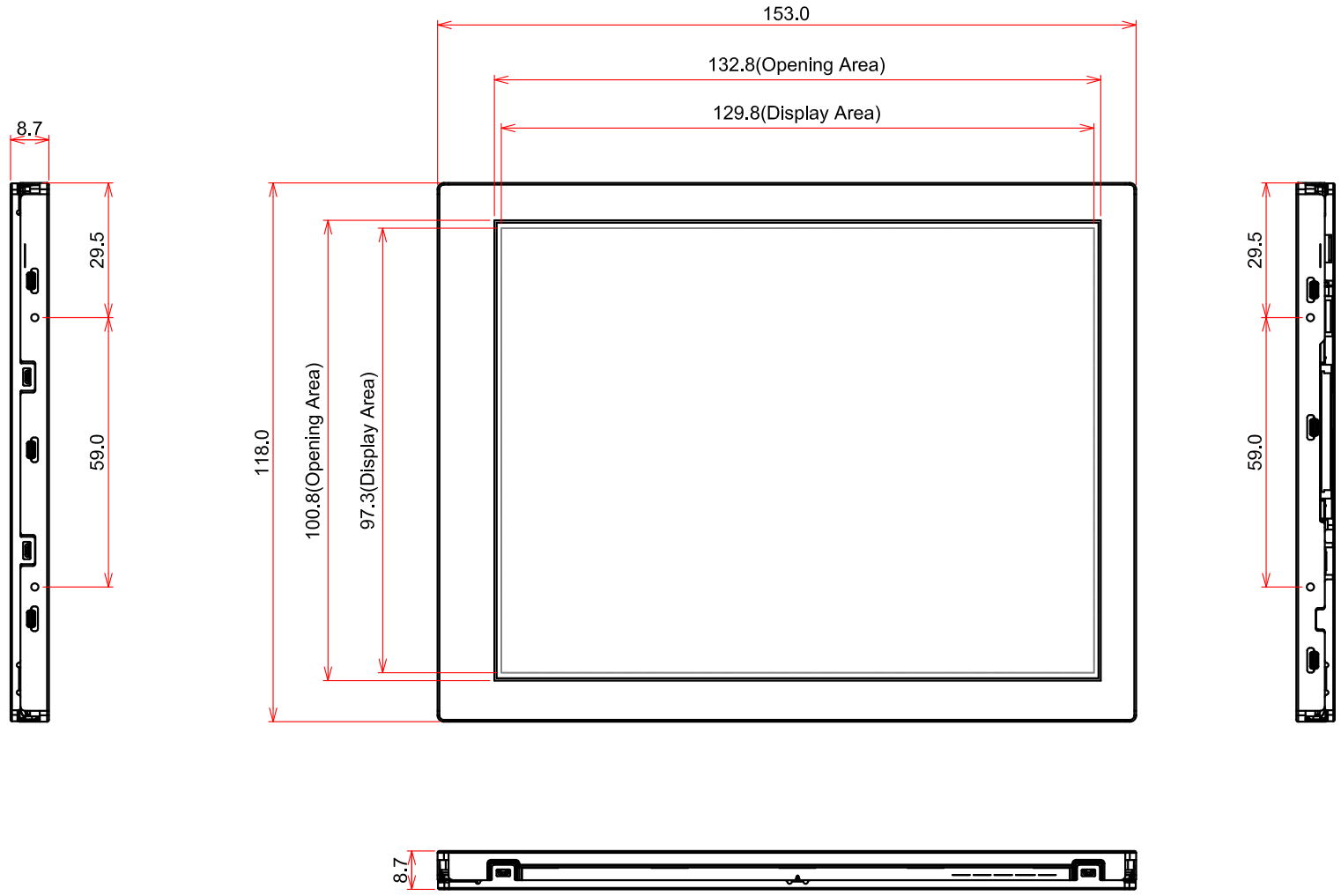
Note 4: In order to avoid any damages, the interval time from power off to power on shall be 1 second minimum.

Note 5: In order to avoid high Inrush current, V_{DD} & V_{LED} rising time need to set at

$0.5ms < V_{DD} \& V_{LED} < 10ms$.

9. OUTLINE DIMENSIONS

9.1 FRONT VIEW

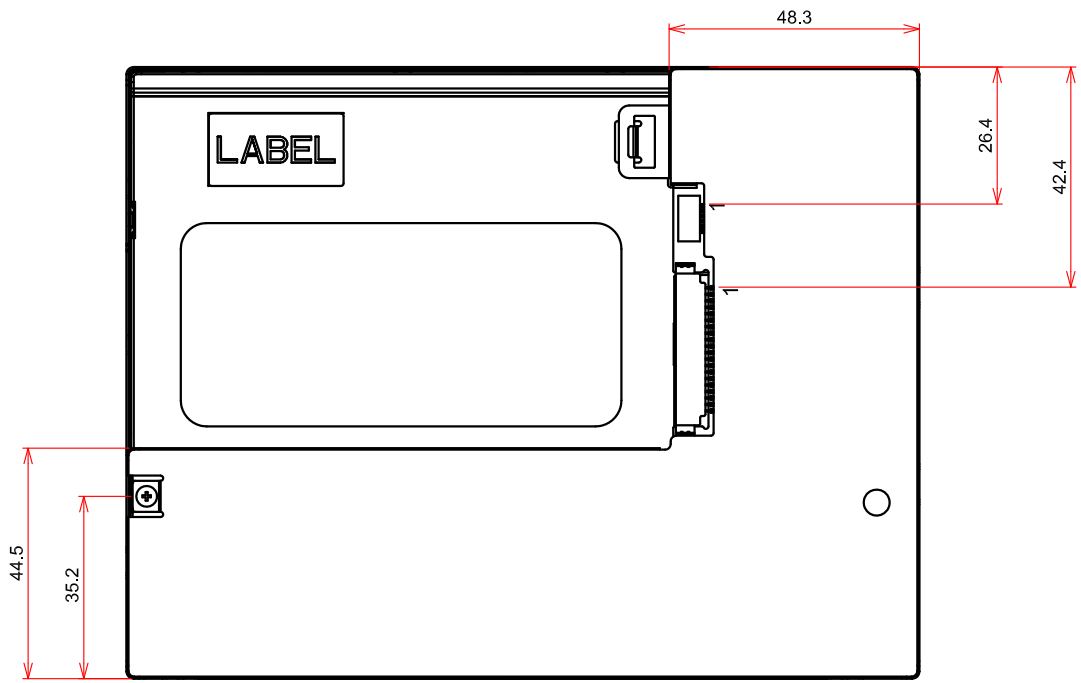


Note 1: Within 0.147Nm (1.5kgfcm) of M2 screw torque is recommed.

General Tolerance:±0.5mm
Scale : NTS
Unit : mm

KAOHSIUNG OPTO-ELECTRONICS INC.	SHEET No.	7B64LTD-2567-1	PAGE	9-1/2

9.2 REAR VIEW



General Tolerance:±0.5mm
Scale : NTS
Unit : mm

KAOHSIUNG OPTO-ELECTRONICS INC.	SHEET No.	7B64LTD-2567-1	PAGE	9-2/2